Experiment #**4**

Accelerator and Wrappers

Kamyar Rahmani

810199422

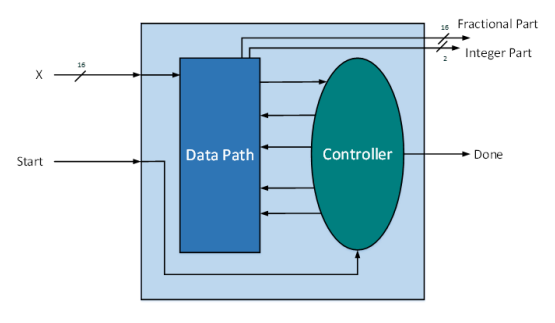
Mohammad Mashreghi

810199492

Abstract**— In this document, we are going to design an Exponential Accelerator Wrapper. For this design first we are going to design its controller and then implement our full design in Quartus environment and in the end we will implement this Accelerator on FPGA.**

Keywords**— SoC, CP, Accelerator, Exponential Engine, Exponetial Accelerator Wrapper, ROM, FPGA**

1. Introduction

System on Chip is an integrated circuit that integrates multiple components including digital, analog, hardware, and software programs all in a single chip. The main core of an SoC is a processor that handles different computational tasks within the system. In addition to the processor, the system includes memory, Input/Output ports, and accelerators. accelerators are dedicated computation units that usually execute one specific task. This single task needs a smaller and less complicated datapath which leads to a high frequency of operation for the accelerators. This is contrary to CPUs in which millions of operations must be executed within a fixed time interval. This imposes a low frequency of operation for CPUs.

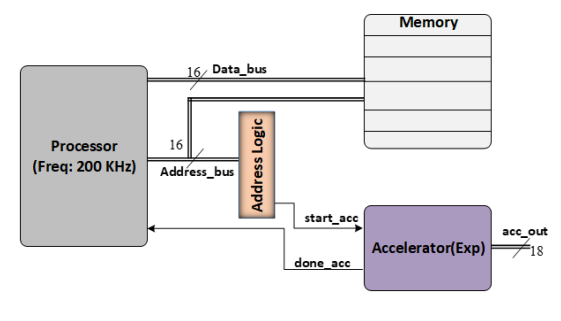


Fig.3 Value of Exponetial for x = 0.25

Fig.1 Block diagram of a typical integrated circuit

1. Exponential Engine

this module receives a 16-bit input ”x” and generates a 16-bit output ”Fractionalpart” and 2-bit ”Integerpart”. The accelerator starts working with a complete pulse on the signal ”start” and when the computation is completed signal ”done” will be sent to the processor to acknowledge it.

Fig.2 Block diagram of exponential accelerator

code examination by running Modelsim simulation :

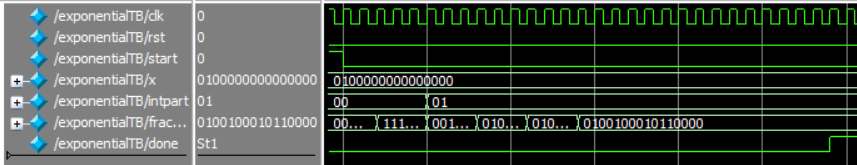
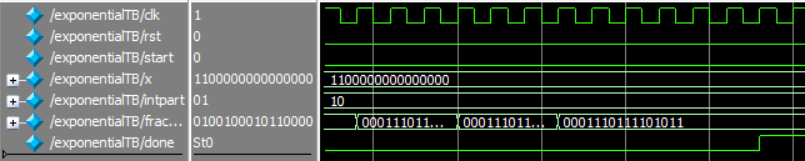
We simulated the code with 3 values of x = 0.25 , 0.75, 0.1875

Fig.4 Value of Exponetial for x = 0.75



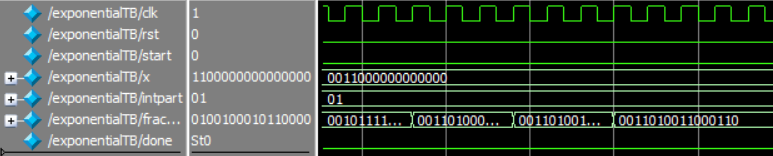


Fig.7 Exponential accelerator wrapper

Fig.5 Value of Exponential for x=0.1875

Design Synthesis

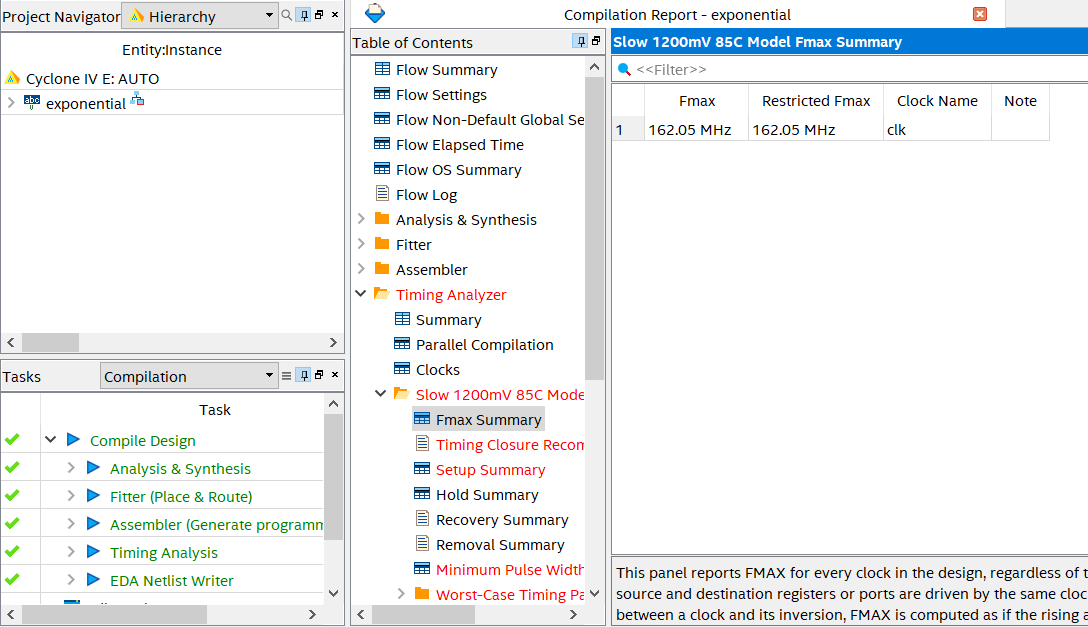
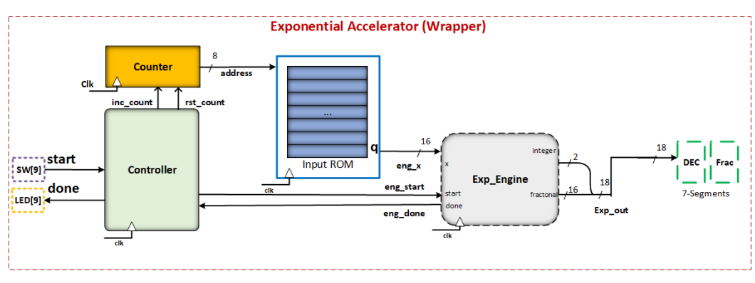
As shown in the figure below, The maximum frequency that this exponential calculator can operate is 162.05 MHz on EP4CE6E22C6 Slow 1200mV 85C and 181.39 MHz on the same device slow 1200mV 0C.

Fig.8 State machine of Exponential Accelerator

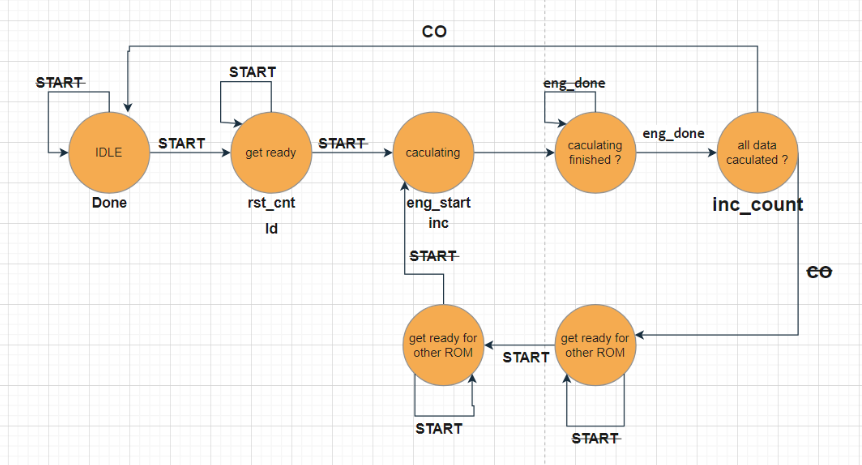
Fig.6 Fmax of Exponential Engine

1. Exponential Accelerator Wrapper

Since the accelerator data will be accessed before and after completing CPU task, the data has to be stored in memory elements in the accelerator wrapper when CPU is busy with other works. The memory element required in this experiment is an input ROM for storing the input data.



The controller in this wrapper is responsible for generating the ”start” signal for exponential engine and the address of each input data reading from the input ROM. The exponential engine should start each calculation when the previous one is completely done. For this purpose ”engdone” is fed to the controller and when done is asserted the controller generates a complete pulse on ”engstart”. At the same time, the correct value of x should appear on the corresponding input of exponential engine. To do this the controller issues the ”inccount” signal for reading data from the ROM. When all calculations are finished the controller sends a done signal on the wrapper output and issues the ”rstcount” signal to reset the counter for the next round of estimations.



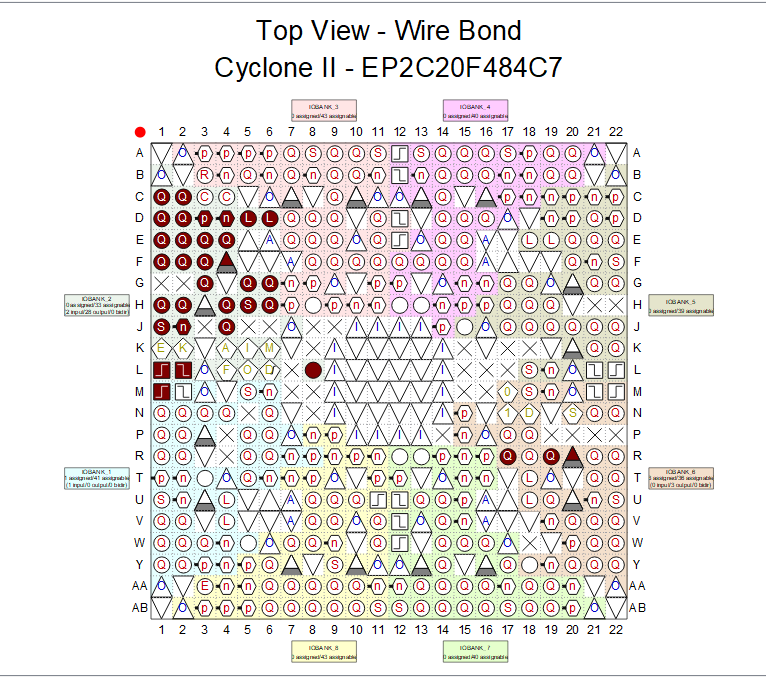
1. Implementing Accelerator on FPGA

Fig.12 Pin Planner

We connected Modules in Quartus as shown in the figure below.

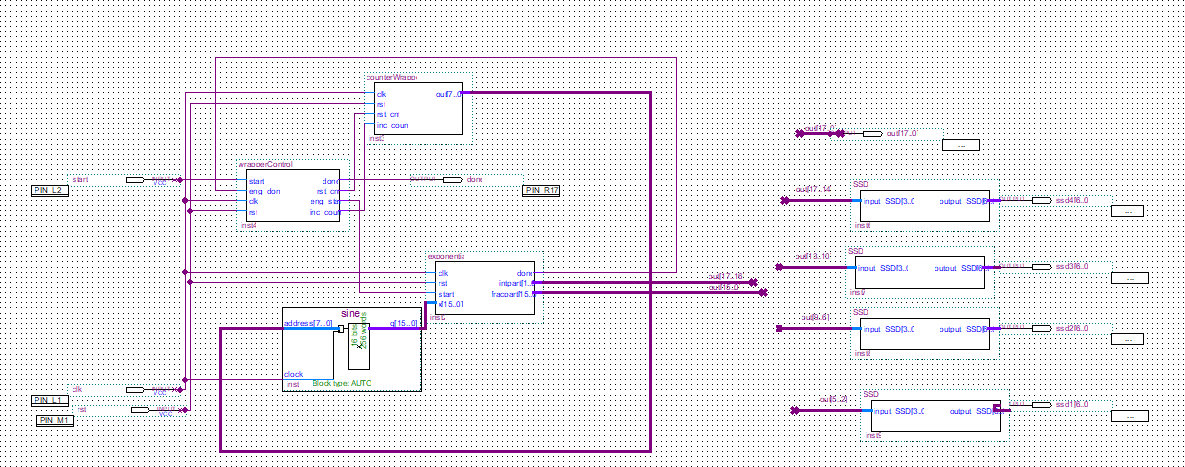
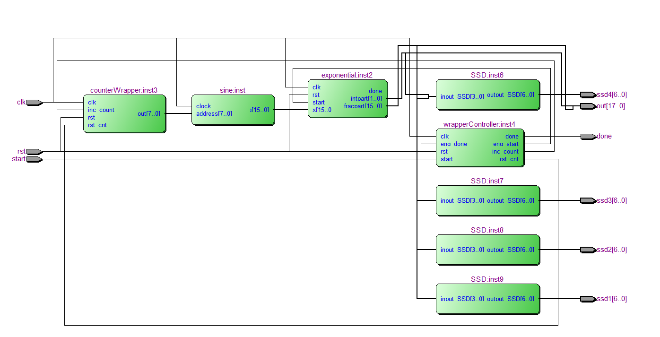


Fig.10 RTL view

Fig.9 Final Design

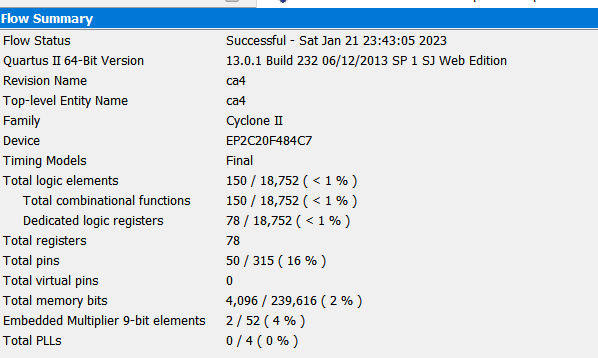


Fig.11 Flow Summary

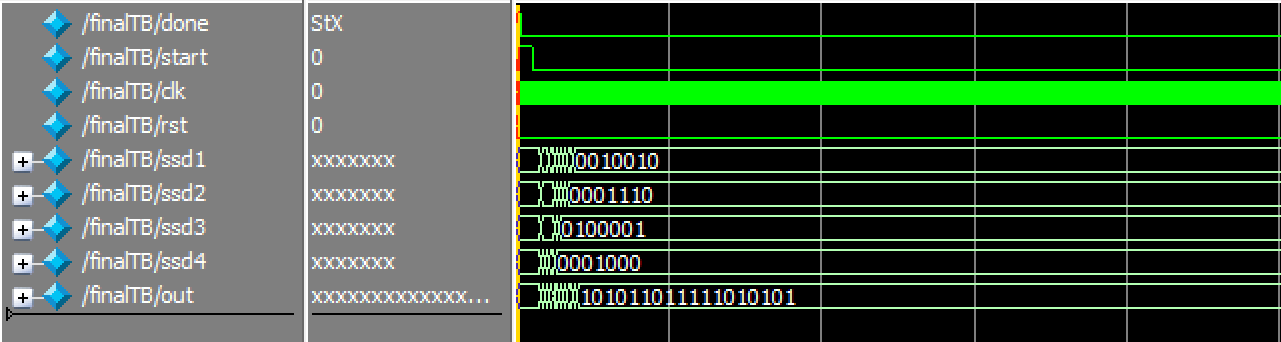
1. Post Synthesis

Fig.13 Fig.4 Value of e^1

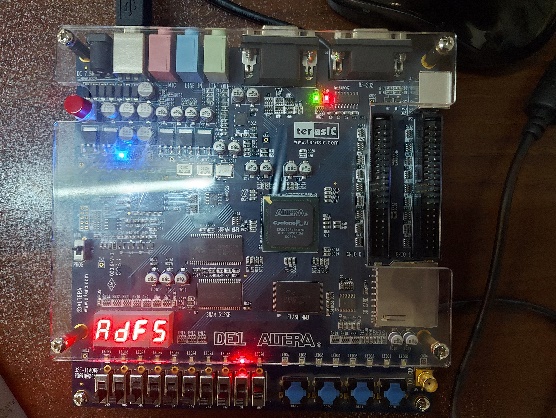


Fig.14 Value of e^1 on Board

On 7-segment we have 16 bits but our fractional part and integer part are 18 bits so we decided to give 2 bit integer and most 14 most significant bits of fractional part to 7-segment.

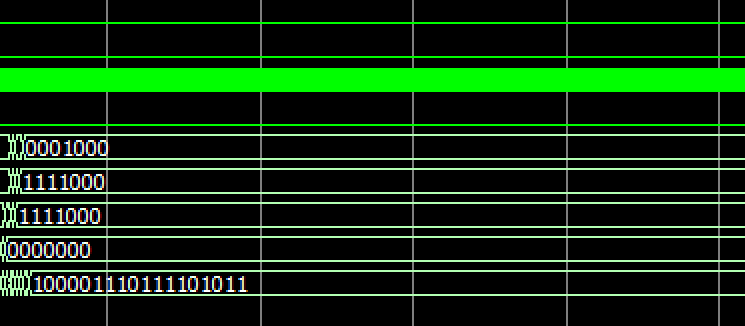


Fig.15 Value of e^0.75

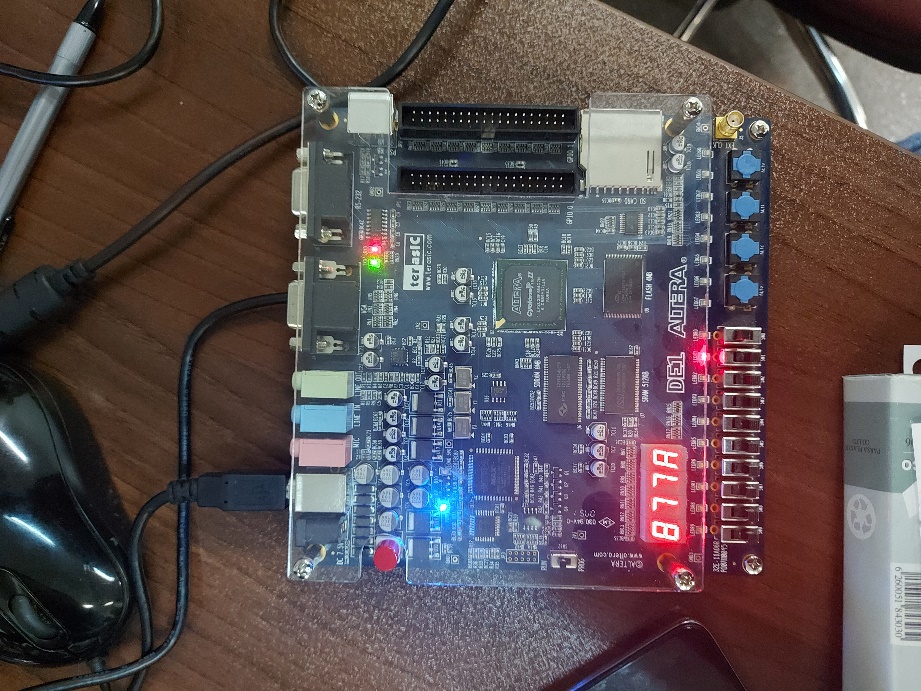


Fig.16 Value of e^0.75 on Board

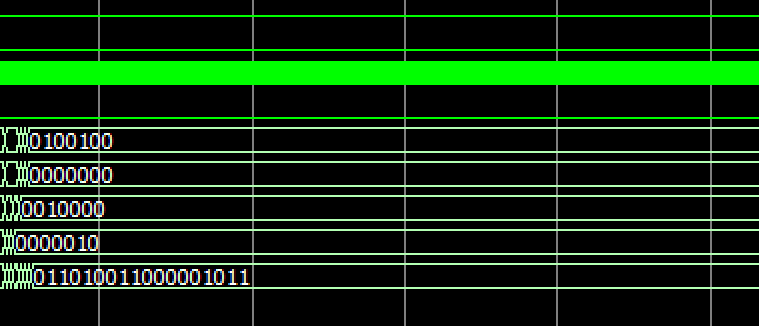
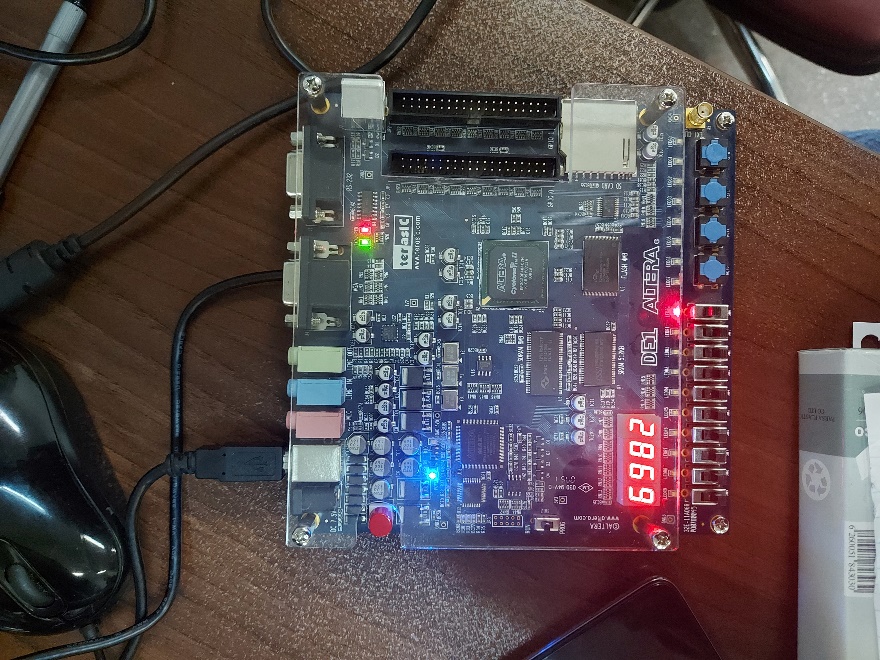


Fig.17 Value of e^0.5

Fig.21 Value of e^0.03125



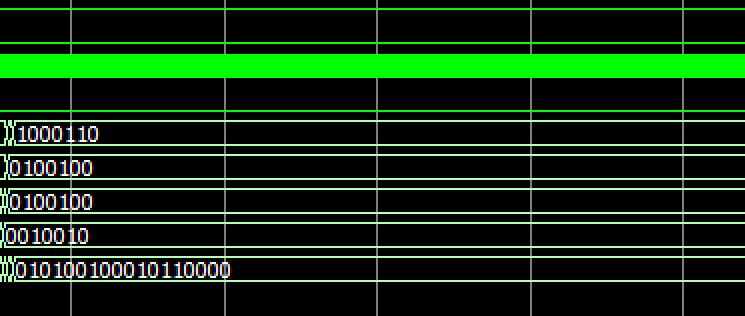


Fig.18 Value of e^0.5 on Board

Fig.19 Value of e^0.25

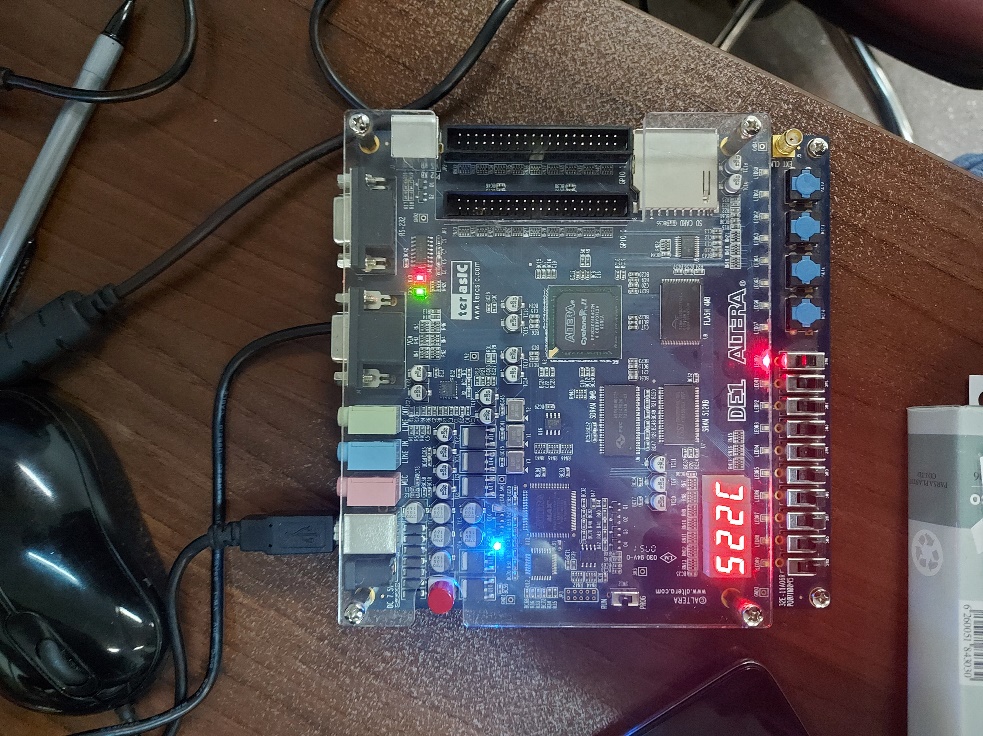
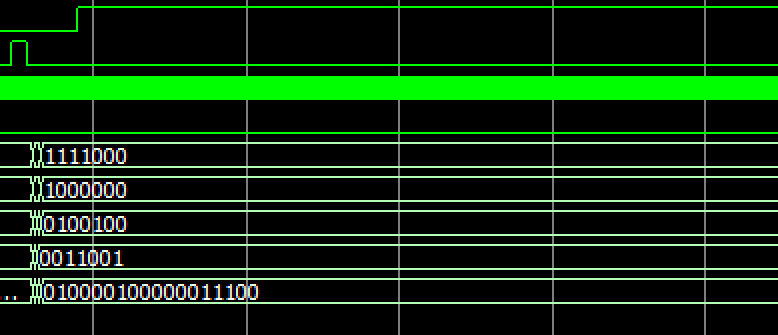


Fig.20 Value of e^0.25 on Board



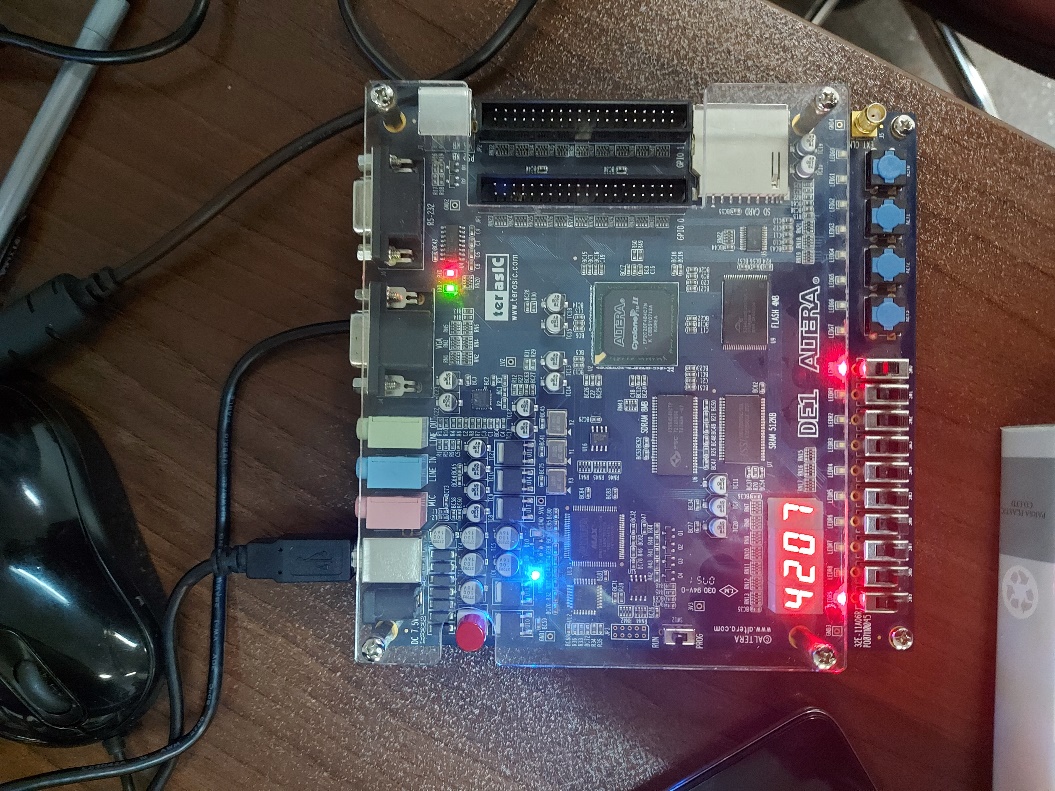


Fig.22 Value of e^0.03125 on Board

1. Conclusion

In this experiment we designed an Exponential accelerator wrapper by designing its controller and implement our circuit in quartus.

and at last we tested our design by implementing it on FPGA board.

1. Refrences

[1] Cyclone II Device Datasheet, Provided by intel.com